

## Nineteenth Annual Single-Event Effects Symposium

# Experimental Characterization of SEE of CMOS 90 nm PLL for the Identification of Dominant Response Circuits

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# Topics

- Milli-Beam Overview and Features
- PLL Block Diagram and Layout
- Milli-Beam Raster Scan of PLL Design
- Correlate PLL Errors to Physical Layout
- PLL Modeling, Dynamics and Jitter
- Measurement of Loss of Lock and Transient Behaviour



# Milli-Beam Overview and Features

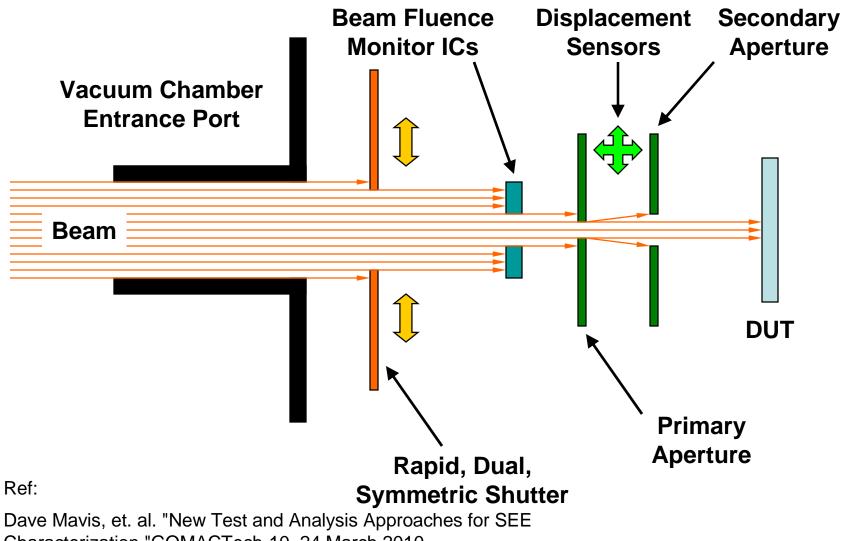
- Precise beam collimation for use at the LBL cyclotron
  - New hardware and software to raster scan complex ICs
  - Achieve spatial resolutions between 5 μm and 500 μm
- Hardware
  - Primary square aperture (2-orthogonal slits) stepped <1 μm precision
  - Secondary scattering cleanup aperture controlled from second stage
  - Displacement sensors provide error feedback signal for corrections
- Software
  - Computes coordinate transformations, sets beam position, controls run
  - Provides FPGA test board with positions for inclusion in error message
- Independent ICs for beam characterization and dosimetry
  - Homogeneous RAM for location and intensity profile measurement
  - Specially designed beam monitor ICs placed upstream of apertures
  - At preset fluences: block the beam, stop data acquisition, step apertures, update FPGA test board with new position, resume data acquisition, unblock the beam

Ref:

Dave Mavis, et. al. "New Test and Analysis Approaches for SEE Characterization,"GOMACTech-10, 24 March 2010

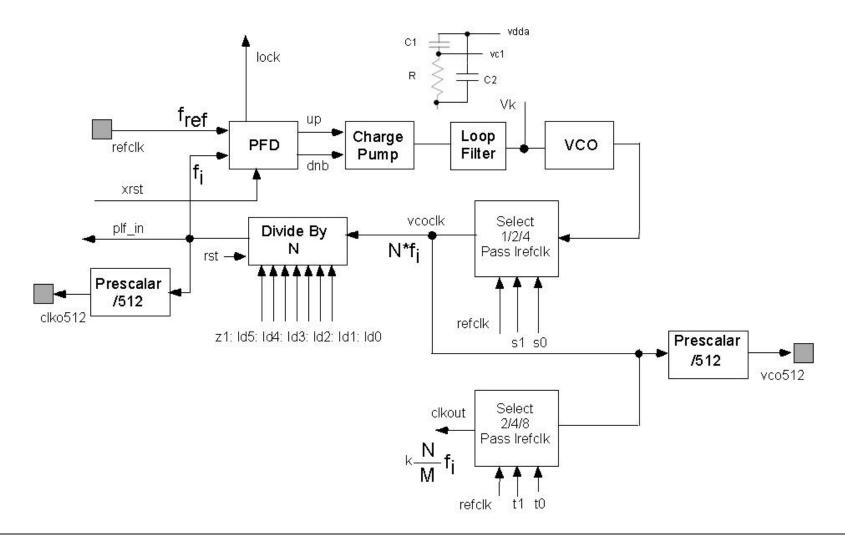


## Milli-Beam Schematic





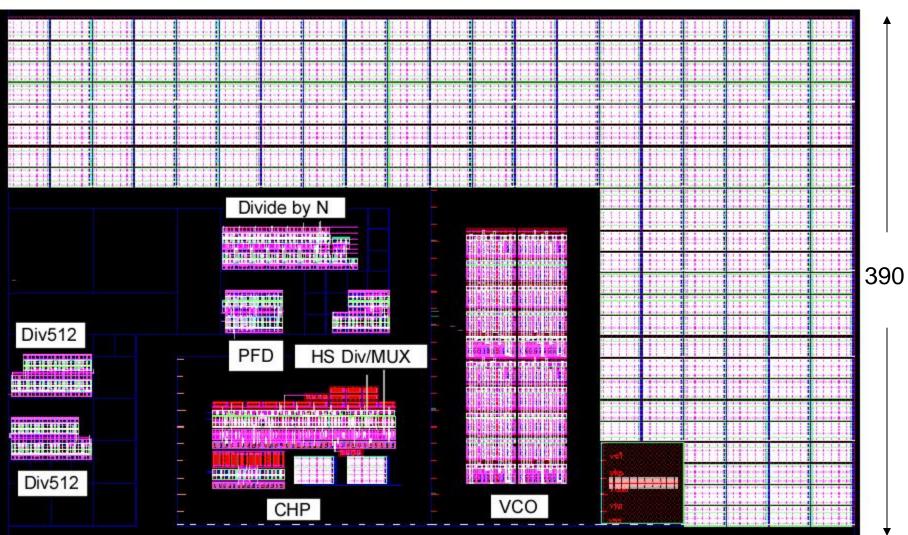
# PLL Block Diagram





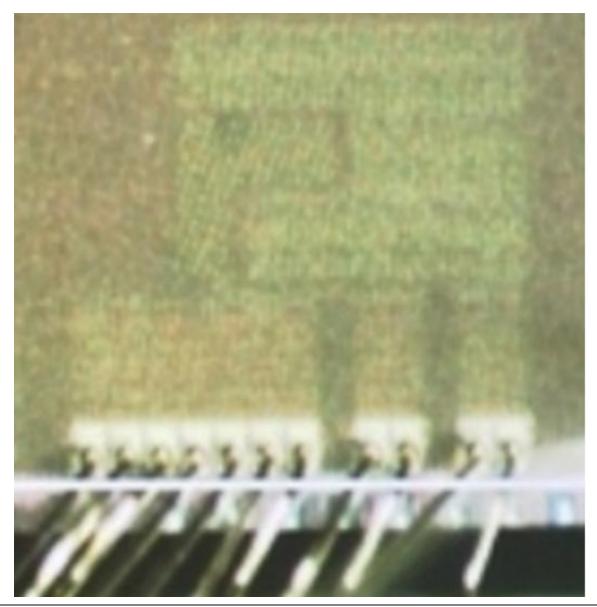
### Micro-RDC PLL Layout IBM 90nm CMOS 9LP Process







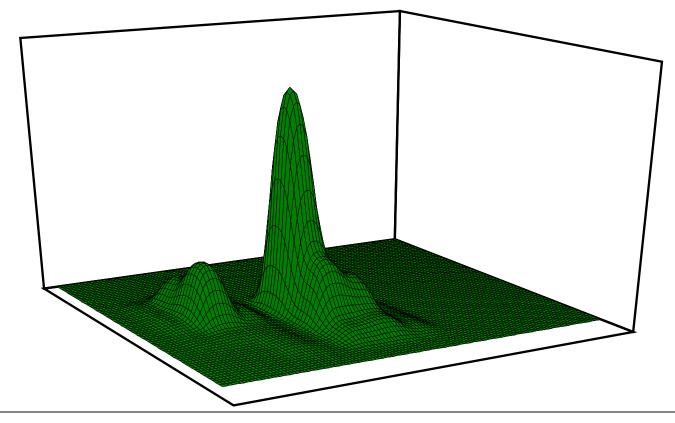
## Micro-RDC PLL Silicon Bonded Out





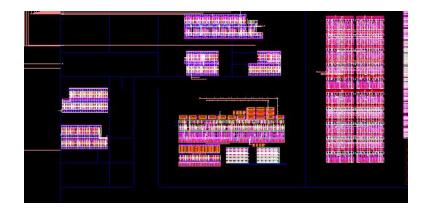
## Raster Scan of PLL Design

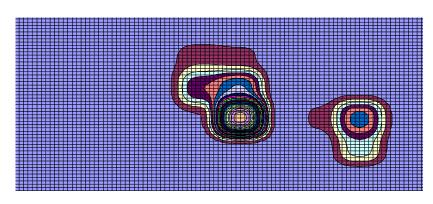
- Scan a 100 µm square beam over the PLL circuitry
  - Better approach than trying to test standalone circuit components
  - Monitor lock signal and measure recovery time
  - Correlate observed errors to specific circuits (CP, VCO, PSD, /N,  $\hat{I}$  M)





# **Correlate PLL Errors to Physical Layout**



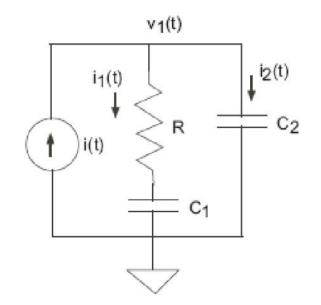


#### **Design Layout**

#### **Milli-Beam Error Contours**



Micro-RDC Microelectronics Research Development Corporation Modeling the Charge Pump for High Level Simulation



Hanumolu, P.K.; Brownlee, M.; Mayaram, K.; Un-Ku Moon, "Analysis of charge pump phase-locked loops", Circuits and Systems I: Regular Papers, *IEEE Transactions on Circuits and Systems* I: Fundamental Theory and Applications, Volume 51, Issue 9, Date: Sept. 2004, Pages: 1665 – 1674



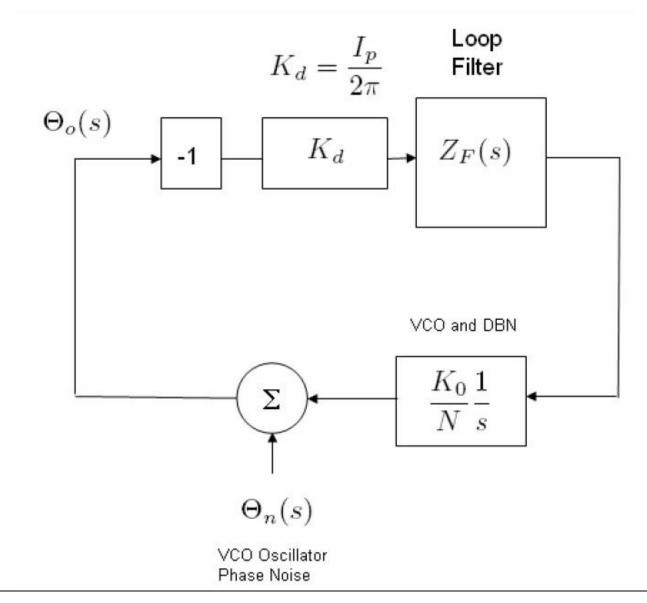
# **PLL Dynamics**

The PLL bandwidth can be defined in terms of the loop gain

$$K = \frac{K_0 I_p R_1}{2\pi N}$$



### **PLL Jitter Analysis**





## PLL Jitter

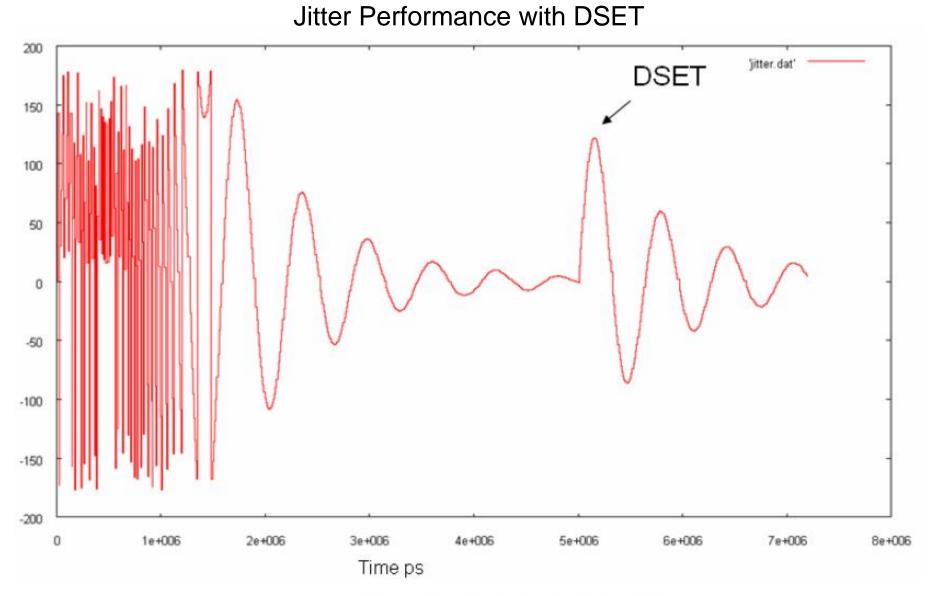
The rms jitter in the synthesized clock

$$\begin{split} \sqrt{E[\Theta_{tot}^2(nT)]} &= \sqrt{\frac{1}{2K_LT}} \frac{2\pi\Delta\tau_{rms}}{T} \\ K_L &= \frac{K_0 I_p R_1}{2\pi N} \\ T \\ \text{Reference Clock Period.} \end{split}$$

The VCO jitter due to VCO phase noise  $\Delta \tau_{rms}$ 

Beomsup Kim; Weigandt, T.C.; Gray, P.R. ,**PLL/DLL system noise analysis for low jitter clock synthesizer design**, *IEEE International Symposium on Circuits and Systems*, 1994. ISCAS '94., 1994 Volume 4, Date: 30 May-2 Jun 1994, Pages: 31 - 34 vol.4

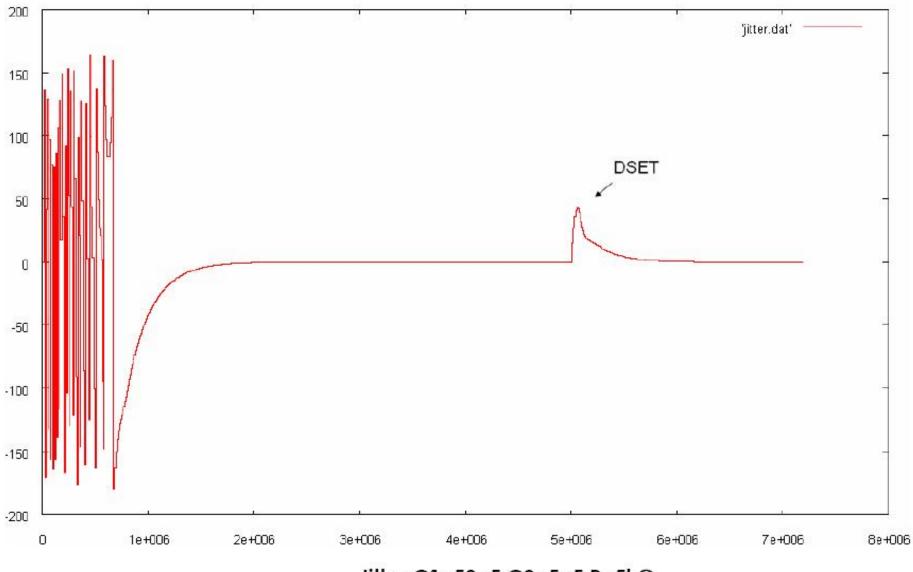




Jitter C1=50pF C2=5pF R=0.5kΩ



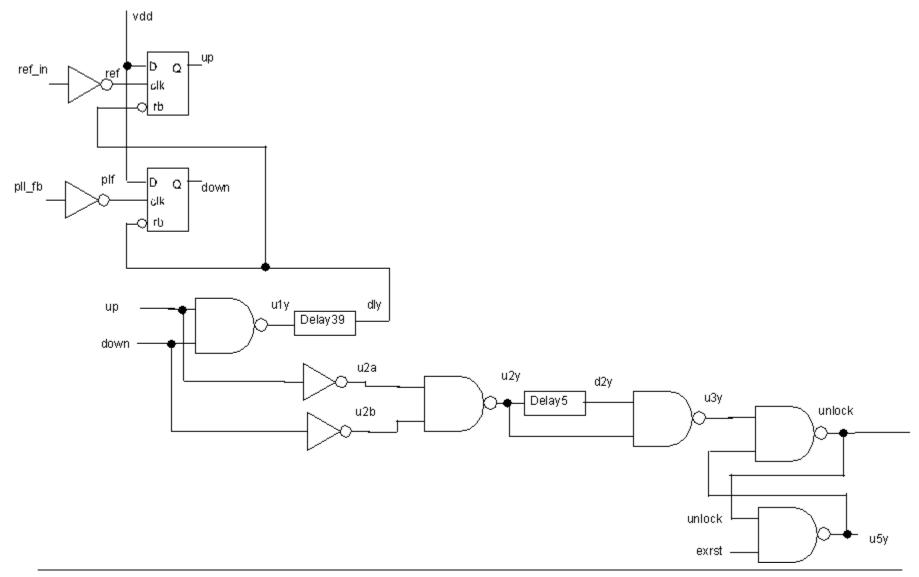
#### Jitter Performance with DSET High Bandwidth



Jitter C1=50pF C2=5pF R=5kΩ

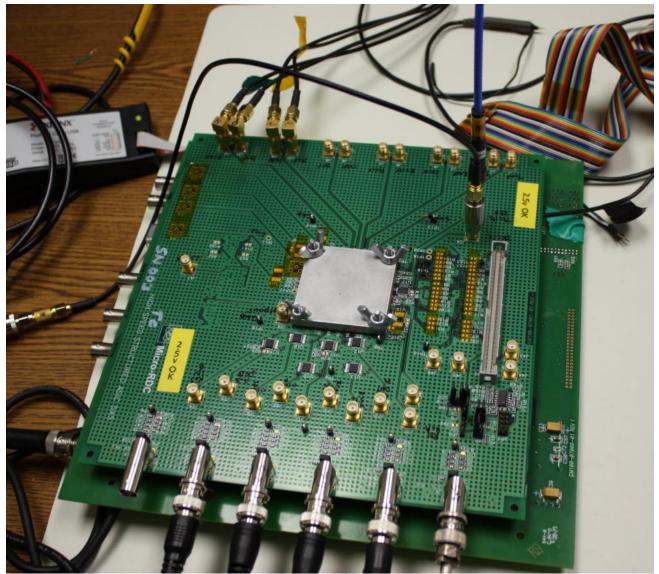


## Lock Detection with Transparent Mode





### High Speed Daughter Card



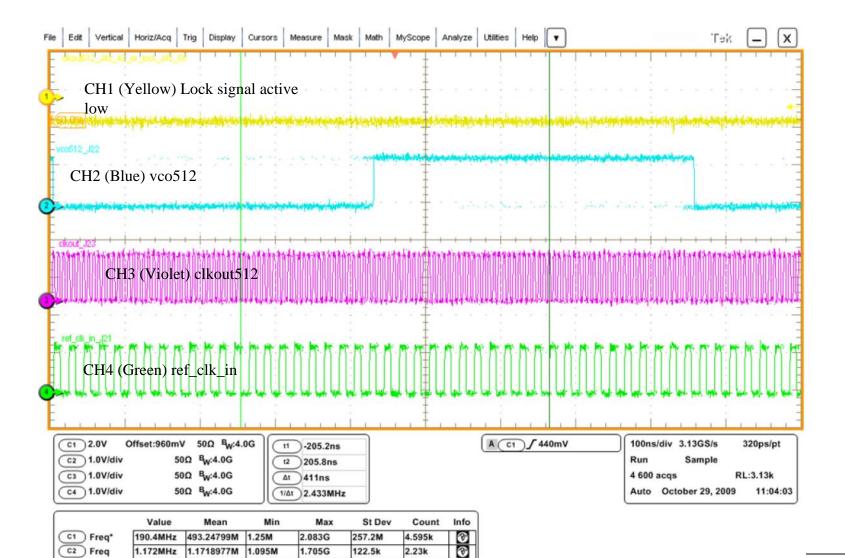


# Scope Screen Capture of the Outputs of 90nm PLL During a Lock Recovery after Switching LD0 High to Low at 50MHz.

File Edit Vertical Horiz/Acq Trig Display Cursors Mea	sure Mask Math M	lyScope Analyze	Utilities Help	X _ XeT
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<u> </u>	9.75M 0.0	1.0		
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	51.5M 0.0 0.09M 0.0	1.0 1.0		



### Scope Screen Capture of the Outputs During a Lock Condition at 50MHz



122.5k

973.6k

104.2k

1.705G

305.8M

50.38M

2.23k

4.6k

4.6k

1

8

49.99MHz 49.999791M

1.1718977M

149.93958M

1.095M

24.75M

49.68M

1.172MHz

148.0MHz

C3 Freq

C4 Freq