Micro-RDC
Microelectronics Research Development Corporation

Nineteenth Annual Single-Event Effects Symposium

Experimental Characterization of SEE of CMOS 90 nm PLL for the Identification of Dominant Response Circuits

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Topics

- Milli-Beam Overview and Features
- PLL Block Diagram and Layout
- Milli-Beam Raster Scan of PLL Design
- Correlate PLL Errors to Physical Layout
- PLL Modeling, Dynamics and Jitter
- Measurement of Loss of Lock and Transient Behaviour

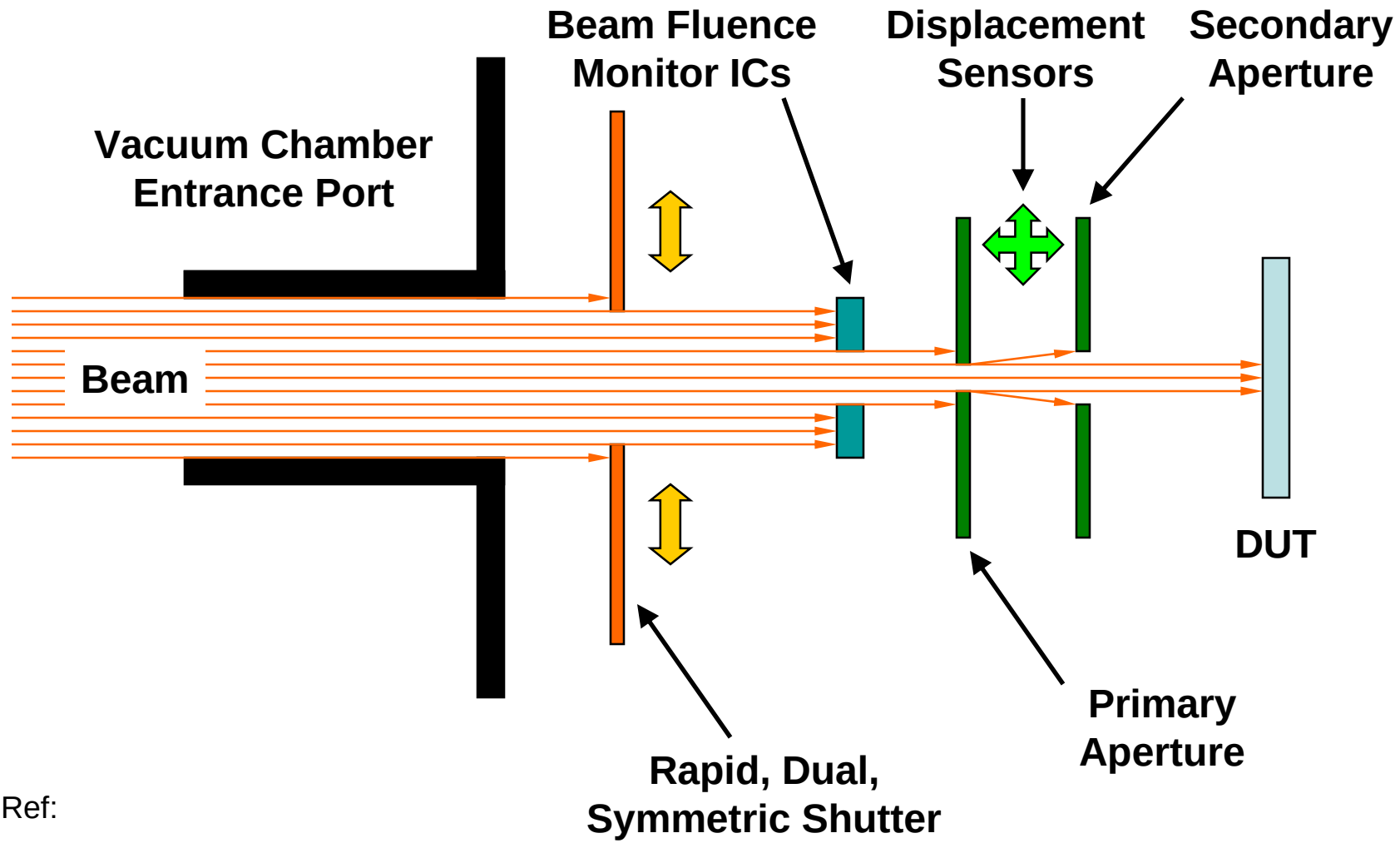
Milli-Beam Overview and Features

- **Precise beam collimation for use at the LBL cyclotron**
  - **New hardware and software to raster scan complex ICs**
  - **Achieve spatial resolutions between 5 µm and 500 µm**
- **Hardware**
  - **Primary square aperture (2-orthogonal slits) stepped <1 µm precision**
  - **Secondary scattering cleanup aperture controlled from second stage**
  - **Displacement sensors provide error feedback signal for corrections**
- **Software**
  - **Computes coordinate transformations, sets beam position, controls run**
  - **Provides FPGA test board with positions for inclusion in error message**
- **Independent ICs for beam characterization and dosimetry**
  - **Homogeneous RAM for location and intensity profile measurement**
  - **Specially designed beam monitor ICs placed upstream of apertures**
  - **At preset fluences: block the beam, stop data acquisition, step apertures, update FPGA test board with new position, resume data acquisition, unblock the beam**

Ref:

Dave Mavis, et. al. "New Test and Analysis Approaches for SEE Characterization,"GOMACTech-10, 24 March 2010

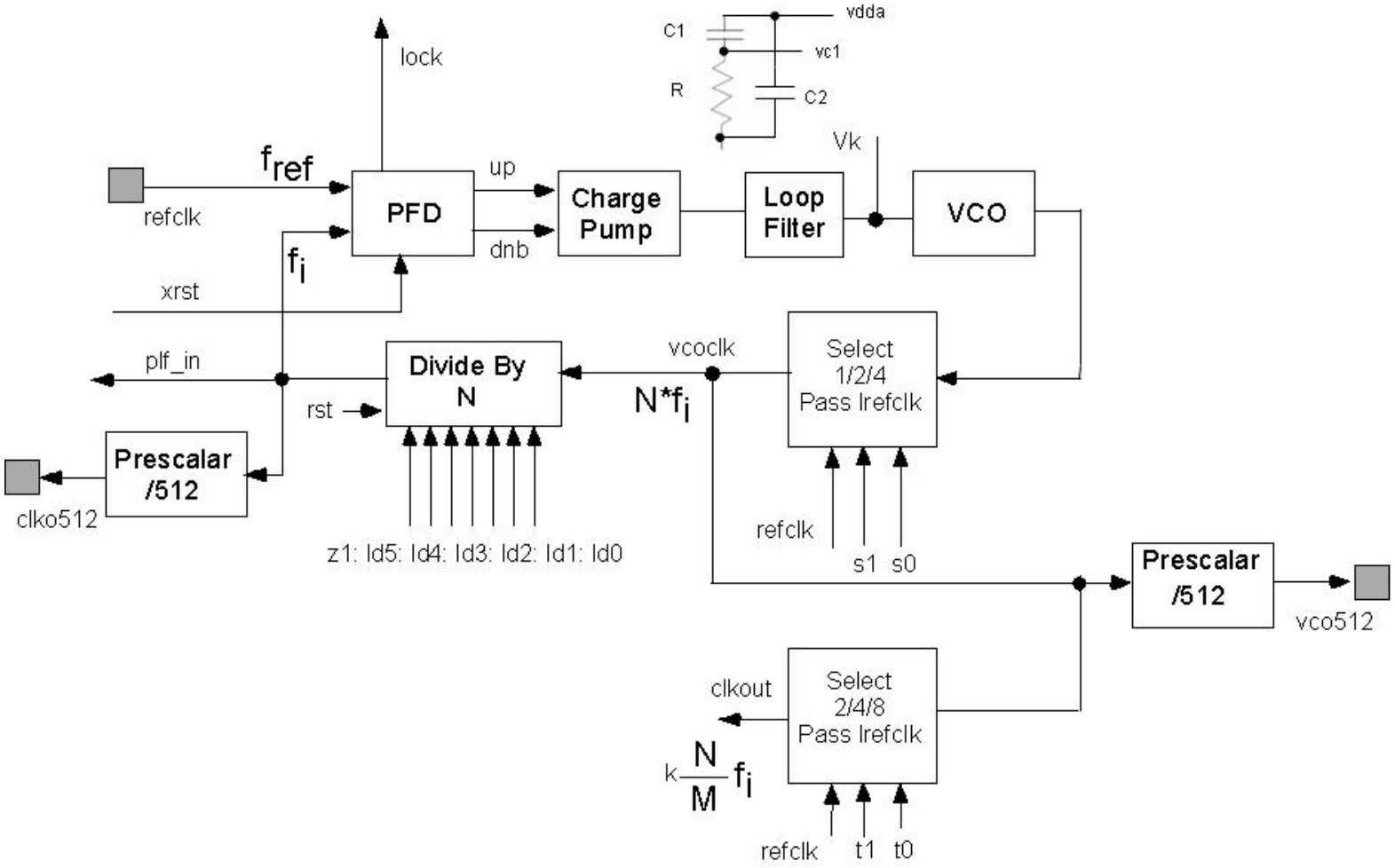
Milli-Beam Schematic



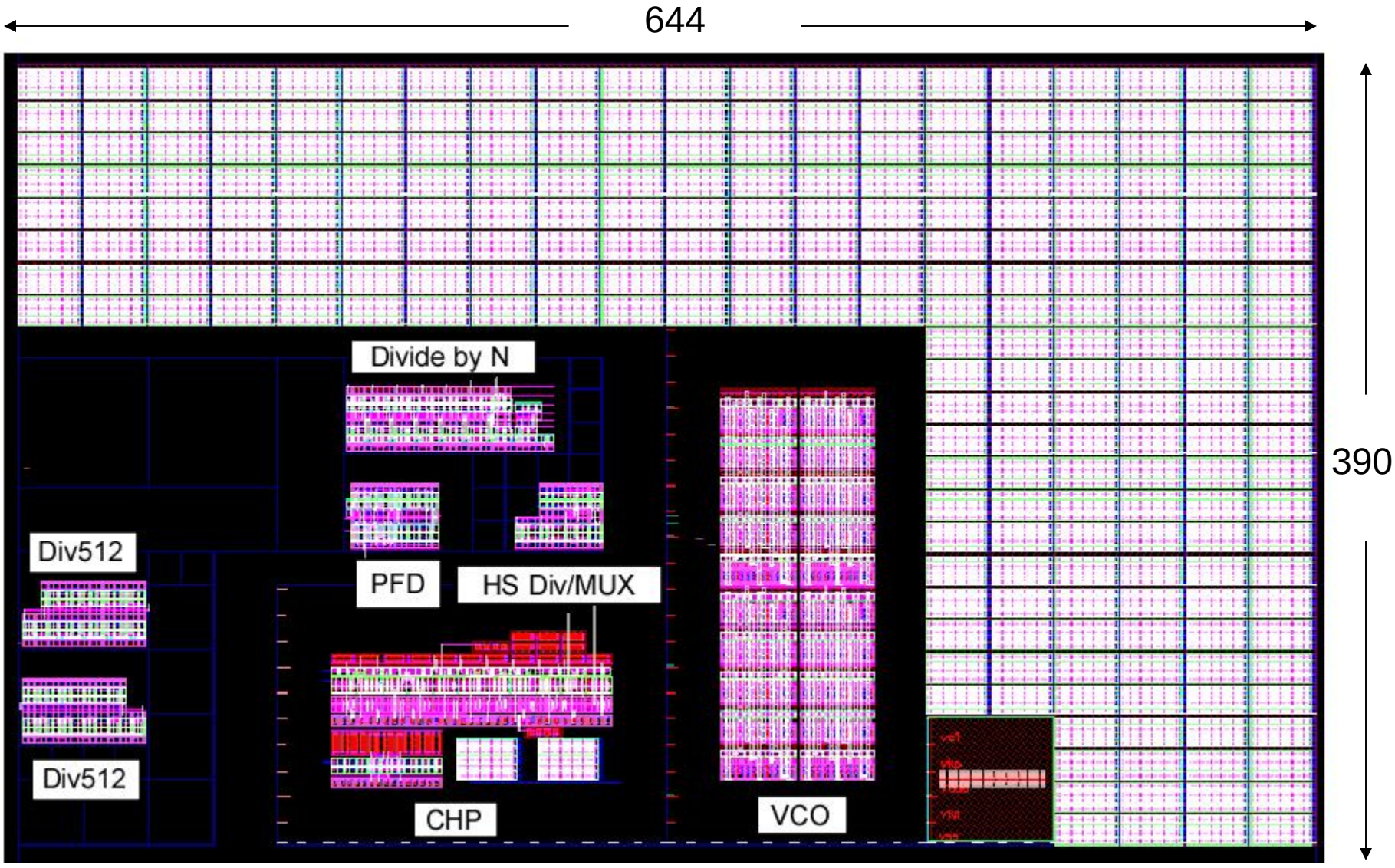
Ref:

Dave Mavis, et. al. "New Test and Analysis Approaches for SEE Characterization,"GOMACTech-10, 24 March 2010

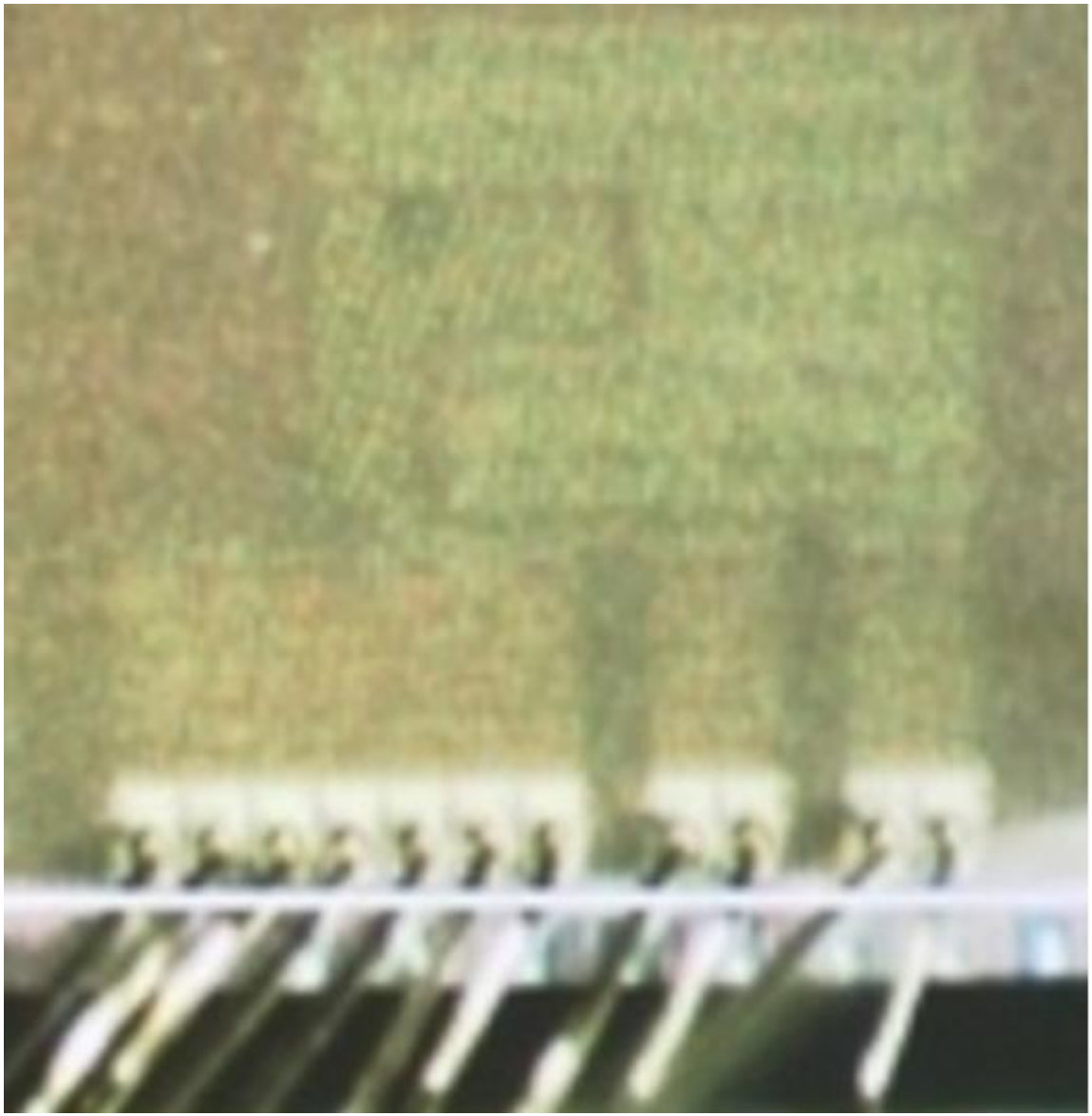
PLL Block Diagram



Micro-RDC PLL Layout
IBM 90nm CMOS 9LP Process

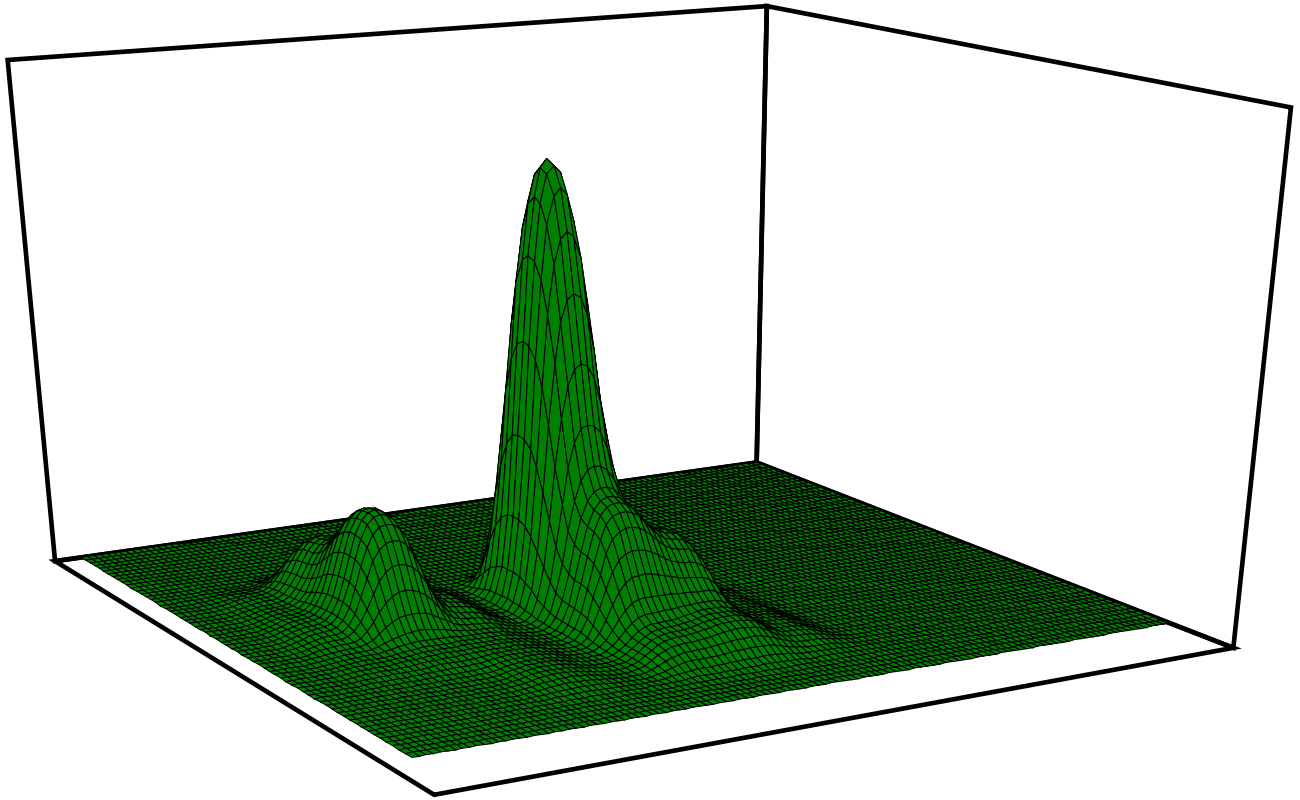


Micro-RDC PLL Silicon Bonded Out

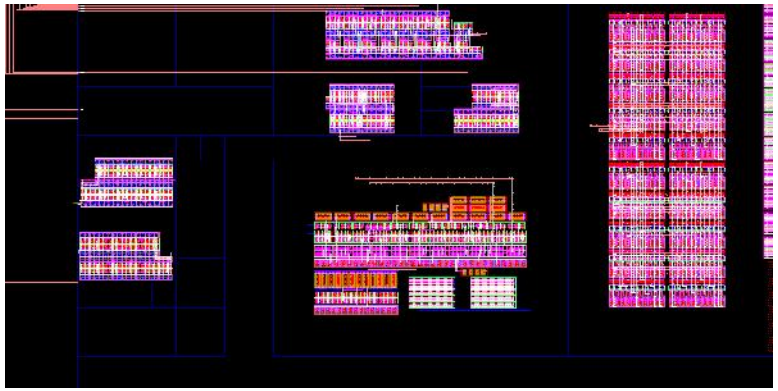


Raster Scan of PLL Design

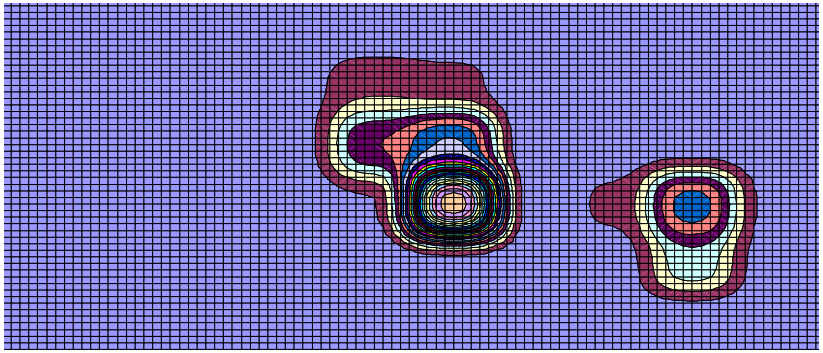
- **Scan a 100 µm square beam over the PLL circuitry**
  - **Better approach than trying to test standalone circuit components**
  - **Monitor lock signal and measure recovery time**
  - **Correlate observed errors to specific circuits (CP, VCO, PSD, /N, òM)**



Correlate PLL Errors to Physical Layout

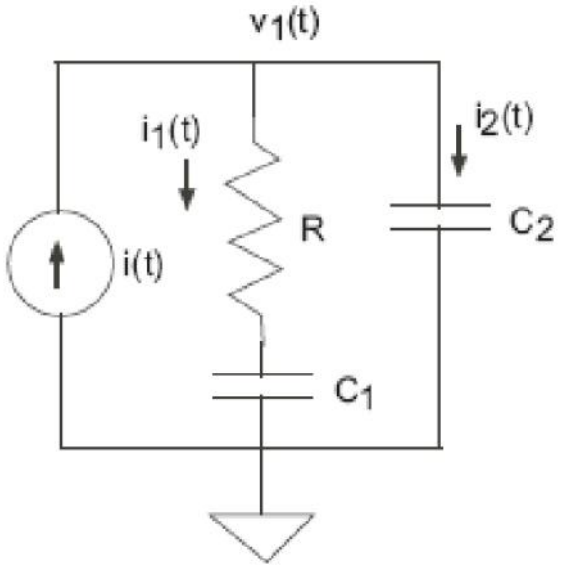


Design Layout



Milli-Beam Error Contours

Modeling the Charge Pump for High Level Simulation



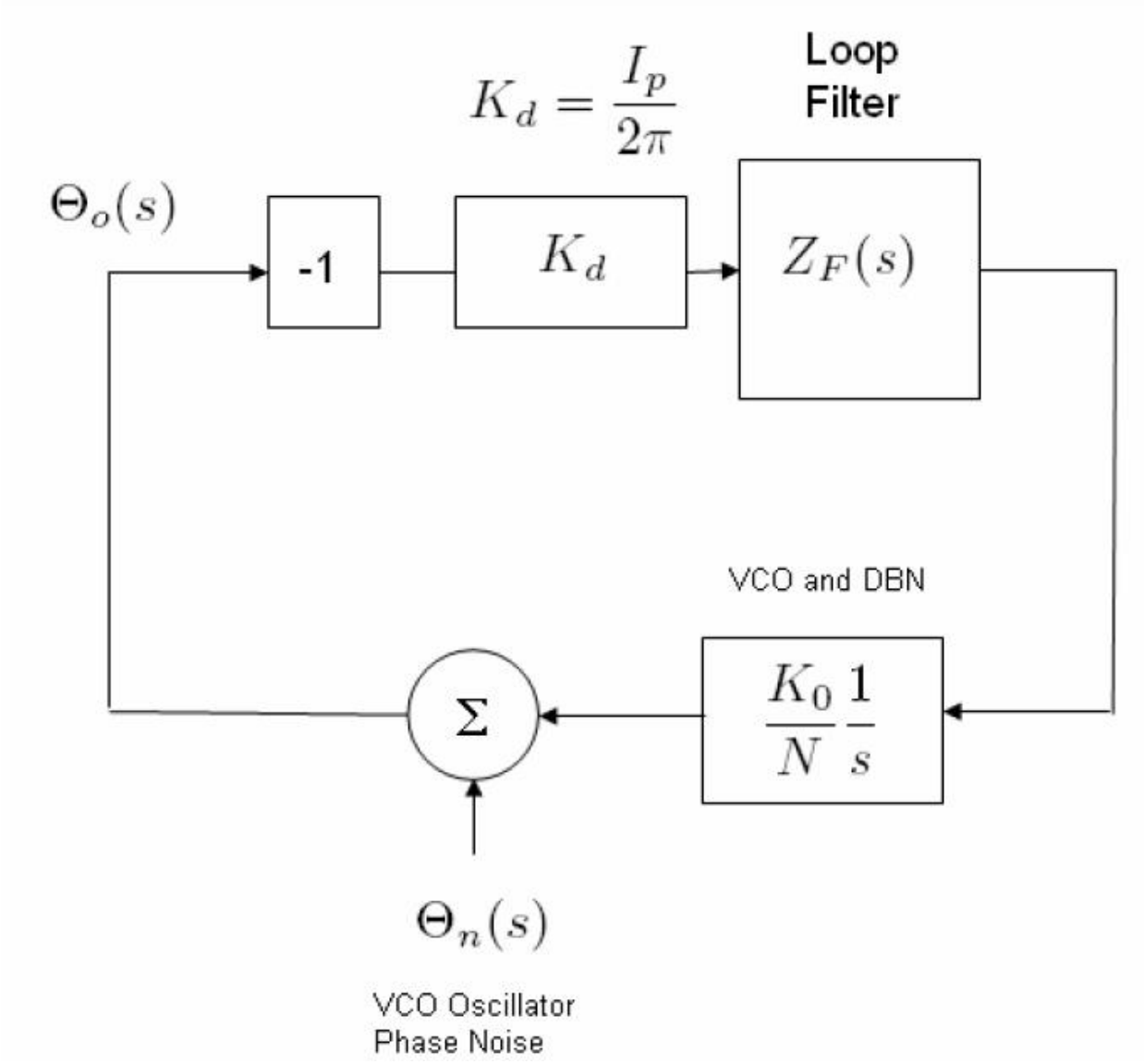
Hanumolu, P.K.; Brownlee, M.; Mayaram, K.; Un-Ku Moon,**"Analysis of charge pump phase-locked loops"**, Circuits and Systems I: Regular Papers, *IEEE Transactions on Circuits and Systems* I: Fundamental Theory and Applications, Volume 51, Issue 9, Date: Sept. 2004, Pages: 1665 – 1674

PLL Dynamics

The PLL bandwidth can be defined in terms of the loop gain

$$K = \frac{K_0 I_p R_1}{2\pi N}$$

PLL Jitter Analysis



PLL Jitter

The rms jitter in the synthesized clock

$$\sqrt{E[\Theta_{tot}^2(nT)]} = \sqrt{\frac{1}{2K_L T}}\frac{2\pi\Delta\tau_{rms}}{T}$$

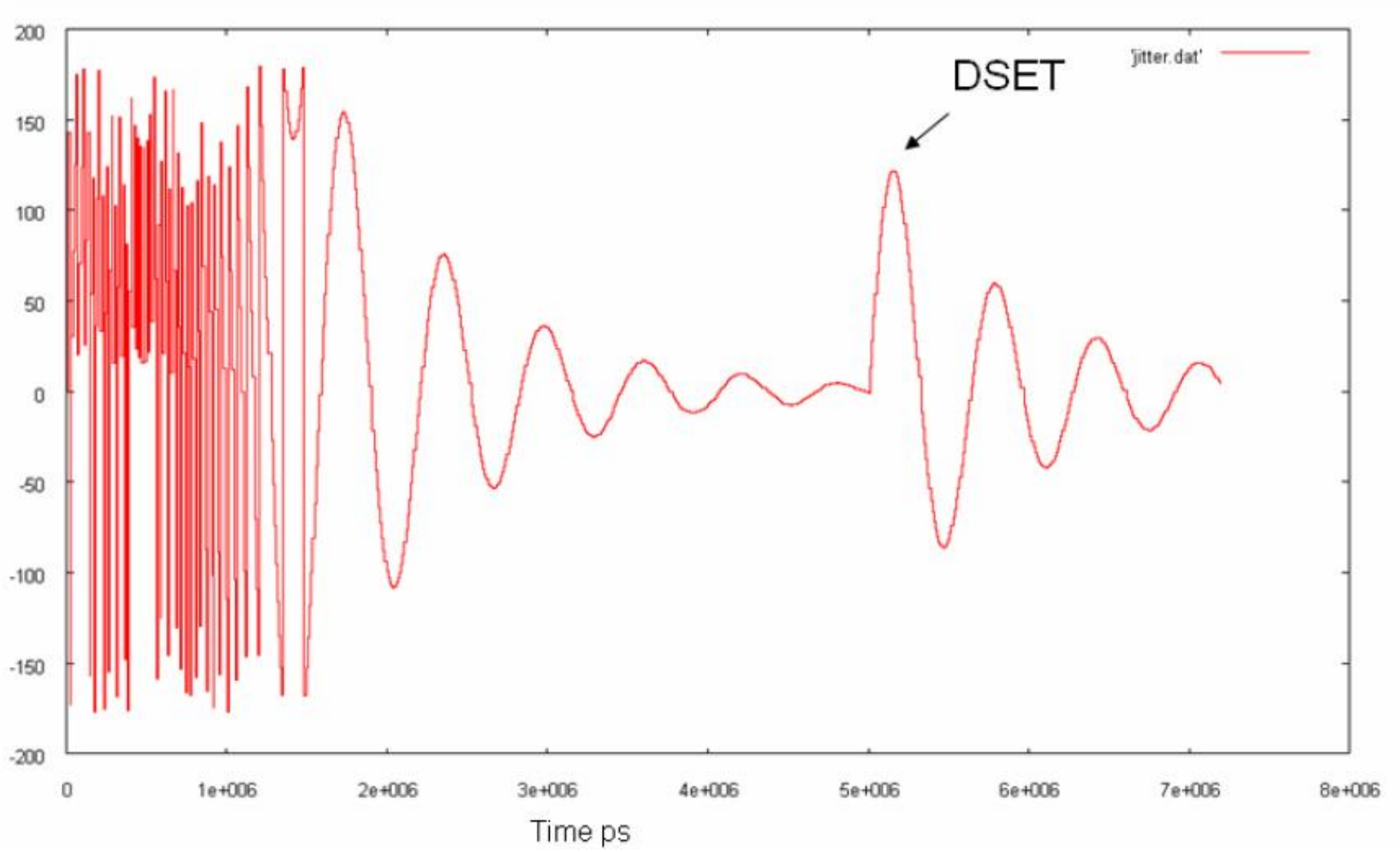
$$K_L = \frac{K_0 I_p R_1}{2\pi N}$$

T Reference Clock Period.

The VCO jitter due to VCO phase noise $\Delta\tau_{rms}$

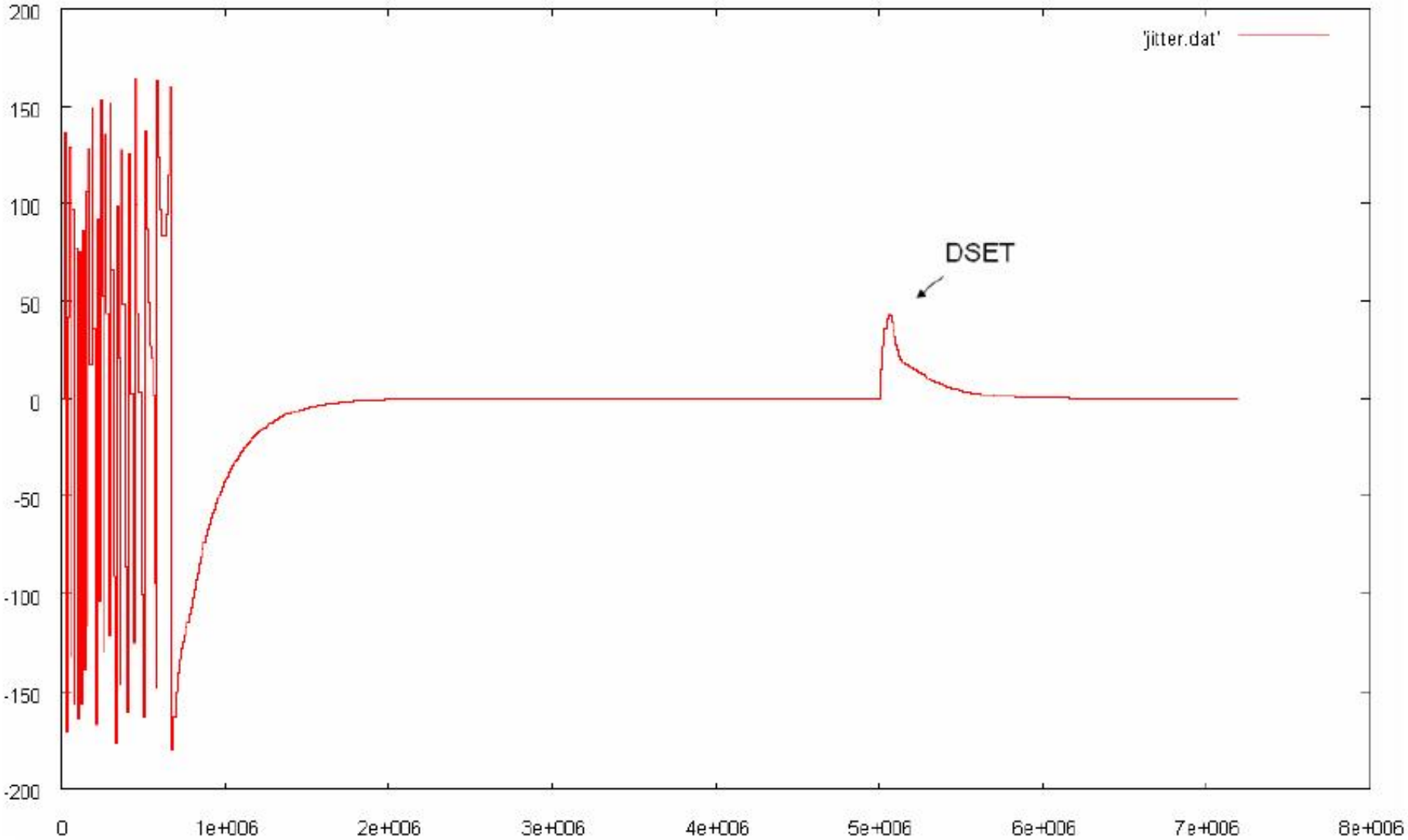
Beomsup Kim; Weigandt, T.C.; Gray, P.R. ,**PLL/DLL system noise analysis for low jitter clock synthesizer design**, *IEEE International Symposium on Circuits and Systems*, 1994. ISCAS '94., 1994 Volume 4, Date: 30 May-2 Jun 1994, Pages: 31 - 34 vol.4

Jitter Performance with DSET



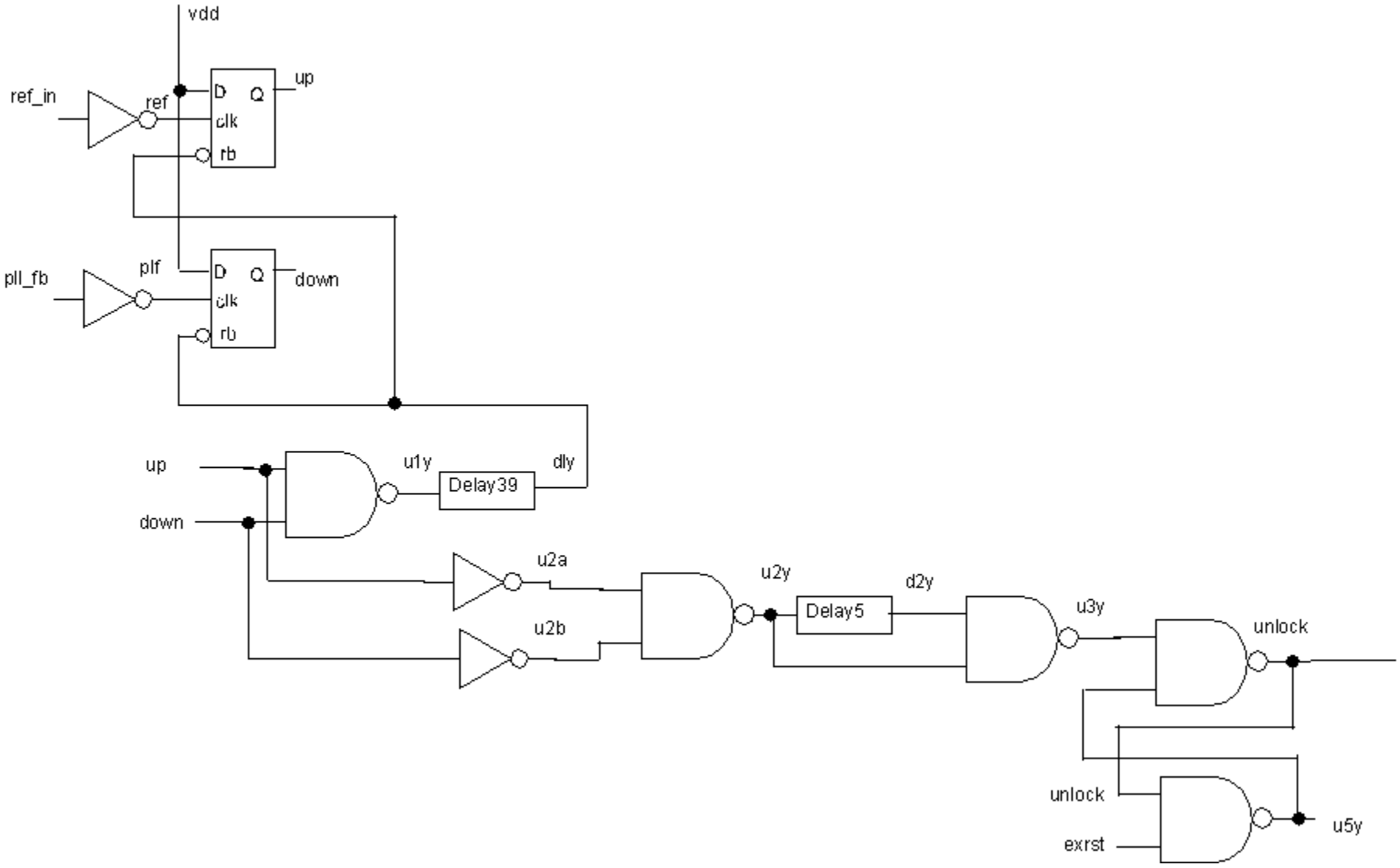
Jitter C1=50pF C2=5pF R=0.5kΩ

Jitter Performance with DSET High Bandwidth

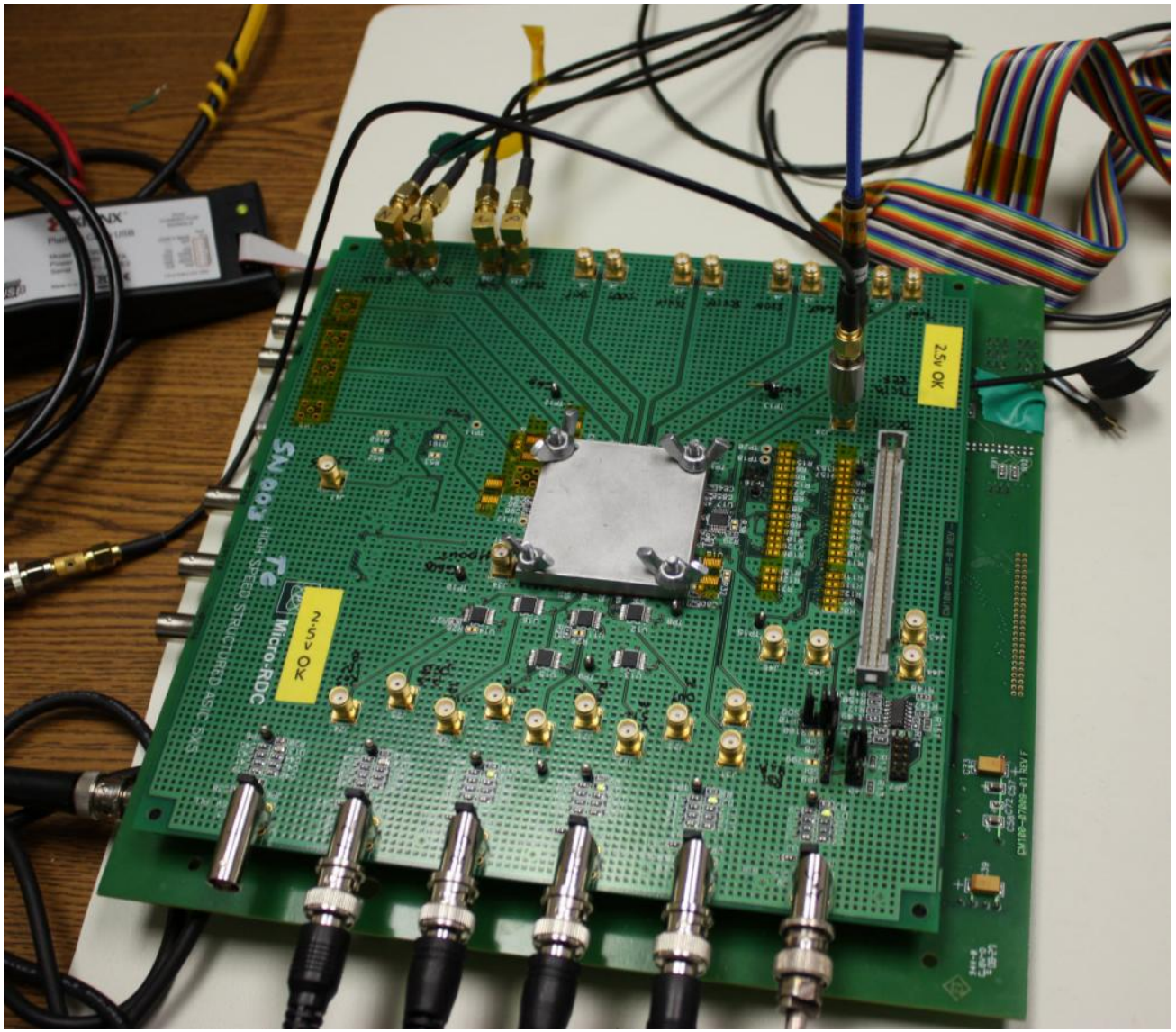


Jitter C1=50pF C2=5pF R=5kΩ

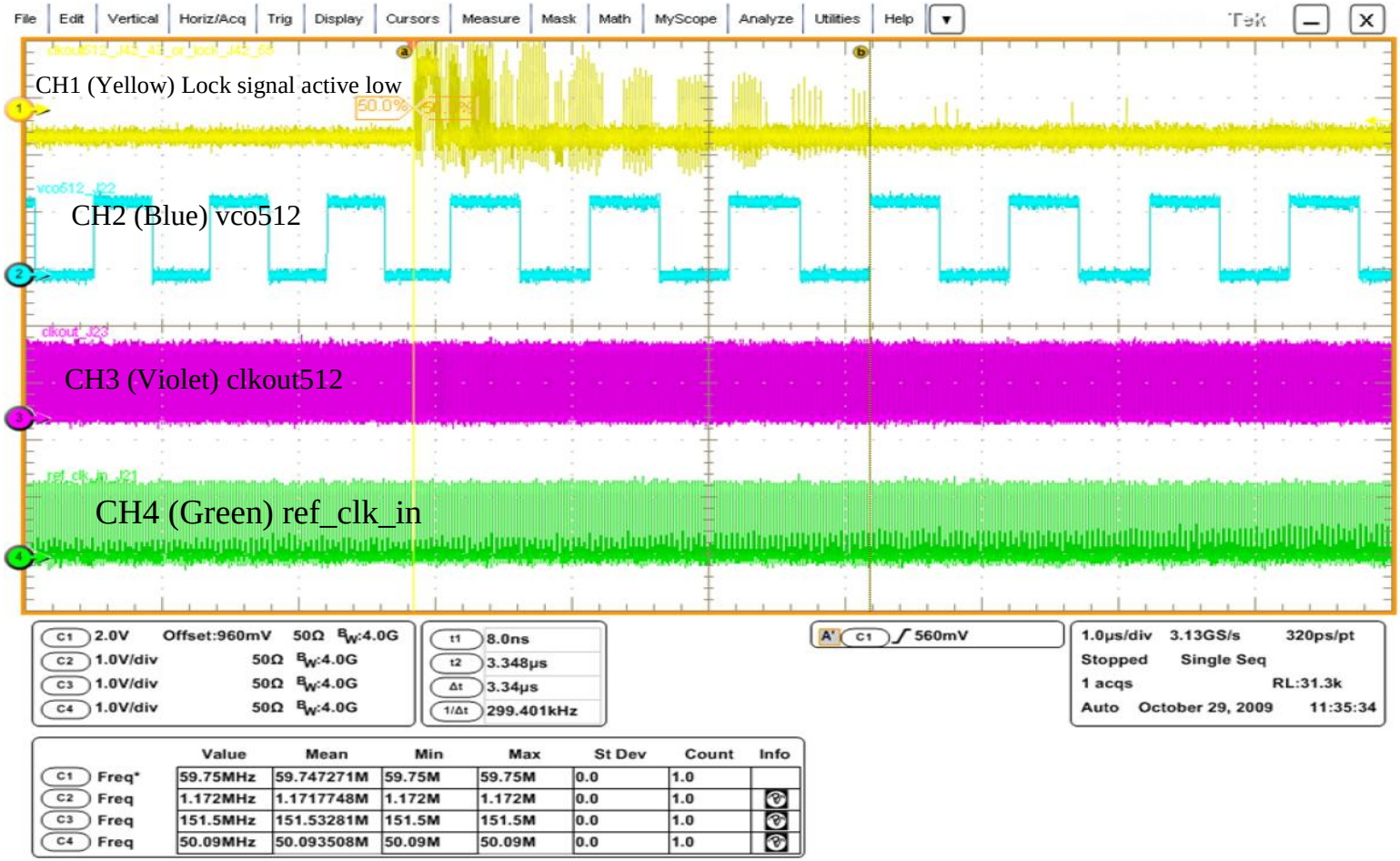
Lock Detection with Transparent Mode



High Speed Daughter Card



Scope Screen Capture of the Outputs of 90nm PLL During a Lock Recovery after Switching LD0 High to Low at 50MHz.



Scope Screen Capture of the Outputs During a Lock Condition at 50MHz