

High Density Interconnect Technology (HDI) for Chip Scale and Land Grid Array Packaging for Space Qualifiable Radiation Hardened Systems on a Chip Solutions

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Abstract: We use the GE High Density Interconnect(POL) Technology to create packages for 7x7mm and 3x3mm die in 90nm Radiation Hardened ASICs. We use HDI to “grow” the 7x7mm,3x3mm die to accommodate existing 1.27mm pitch LGA Packages. Next we create 16x16 and 10x10 BGAs with 0.8mm pitch for ultra small size, high acceleration, temperature cycling for space electronics.

Keywords: HDI;MCM;ASIC;Rad Hard;Packaging; POL;Wire Bond;BGA;Temporal Latch;TID.

Introduction

The design and implementation of Systems on a Chip in the 90nm CMOS process using Radiation Hardened By Design techniques in [Ardalan, 2011]and [Ardalan, Small Sat 2011] results in the integration of the microcontroller, on-chip EDAC protected SRAM and multiple communications and interface cores (Spacewire, USB, SPI, I2C and Serial) along with power management on a single die. The die sizes for the two SoCs are 7x7mm and 3x3 mm. The SoC's support 192 and 96 CMOS I/O respectively. For Spacewire support, on chip LVDS transceivers are provided in addition to the CMOS I/O. A major issue arises in that many existing packages are designed for the larger technology nodes and are not suitable for the small die at 90nm CMOS and beyond. Nor do they accommodate the larger pin count. This creates a major problem in meeting the maximum bond wire length to meet MIL-STD-883. The High Density Interconnect (HDI) process, [Fillion,1995], [Ader, 1991] and [Forman, 1993], at GE allows for multiple packaging challenges to be addressed. For the 90nm CMOS Radiation Hardened by Design ASICs the Radiation Hardness Estimates are:

Total Ionizing Dose: Within Specifications after Exposure to Greater than 1Mrad(Si). **Single Event Latch Up:** Latchup immune to 80 MeV-cm²/mg. **SRAM Error Rate:** Supports Scrubbing Program SRAM to Obtain Desired Error Rates. **Single Event Transient:** Implements the

Temporal Latch Based Flip Flops to Mitigate Transient Pulse Widths of up to 1ns.

Redistribution for Wire Bond

The first challenge is that the HDI process allows us to address, is the ability to “fan out” the die I/O through a new layout such that new larger bond sights are created at the periphery that can accommodate larger diameter bond wires and shorter lengths in turn providing stronger bonds. We have developed HDI layouts that solve this problem for the 7x7 die so that a Ceramic 22x22 LGA package (1.27mm pitch) can be used with the die. This has also been accomplished for the 3x3 die with a 13x13 LGA (LGA 168) package. The new HDI parts allow for the larger cavity LGA packages to be used with the 90nm die and meet the bond wire specifications for Space deployment. See Figure 1 for the LGA packages dimension and size relative to the BGA solutions that will be introduced in a later section. The larger pitch (1.27mm) is also suitable for ease of manufacturing. The LGA 168 and LGA 484 Ceramic Packages have Space Flight Heritage. For Space applications the column attach method for LGA's that has been employed extensively by Six Sigma can be used. See [Winslow, 2005].

To illustrate the redistribution process using HDI, Figure 2 shows the art work for the HDI part illustrating the bond sites of the 3x3mm 90nm Die and the LGA 168 package bonding sites. Note that the HDI part now fits the cavity and also the wire bond lengths are dramatically reduced. See Figure 3. The taped out HDI parts for the Redistribution 3x3mm and 7x7mm Die are shown in Figure 4. The Redistribution bond site dimensions are 100x200 μm with a 190 μm pitch. The 90nm Die have 50x50 μm pad sizes with 64 μm pitch. The Redistribution HDI parts can handle larger diameter bond wires and support much stronger metallurgical bonds than the Aluminum bond sites in the original die.

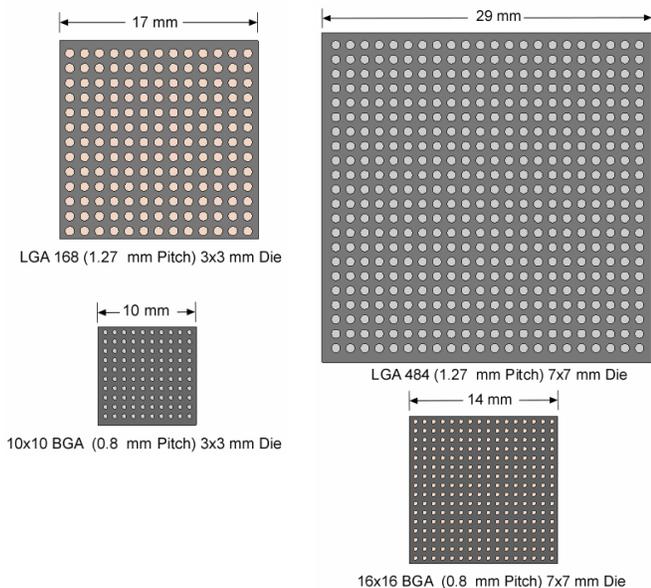


Figure 1 LGA 168 and LGA 484 Packages for the 3x3 mm and 7x7mm Die along with the 10x10 and 16x16 0.8mm Pitch BGAs for the 3x3mm and 7x7mm Die.

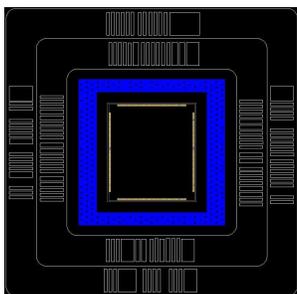


Figure 2 HDI Redistribution Art Work Showing the Die Bond Sites (Pad Pitch 64 μm , Pad 50 μm x 50 μm). The Redistribution Part is shown placed in the LGA 168 package

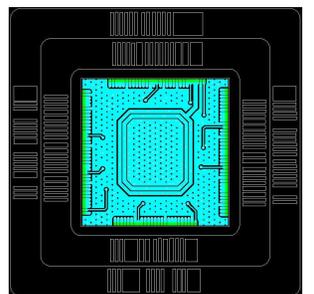


Figure 3 HDI Redistribution Art Work Showing the Redistribution of Bond Sites with Power and Ground Rings

Chip Scale Packaging

The second challenge takes advantage of HDI to develop Chip Scale Packaging (CSP) to achieve a very small package with 0.8 mm pitch that also supports all the CMOS I/O for the two ASIC SoC solutions. In this case, we have gone from the 22x22 pin LGA for the SoC in [Ardalan, 2011] with package dimensions of 29x29mm to a 16x16 grid BGA measuring 14x14mm. For the SoC in [Ardalan Small Sat, 2011], the CSP is a 10x10 array measuring at 10x10 mm. These very small packages eliminate the bond wire issues and also support very high speed interconnects. The smaller size packages pave the way for high performance, low power, and very small size for space applications.

Figure 5 shows the art work for the 16x16 BGA illustrating the bond sites for the 7x7mm Die. The Power (Core and I/O) and Ground signals are consolidated on power rings. The signals from the die are routed to the BGA pins. Figures 6 and 7 show the actual HDI BGA parts for the 3x3mm and 7x7mm ASICs.

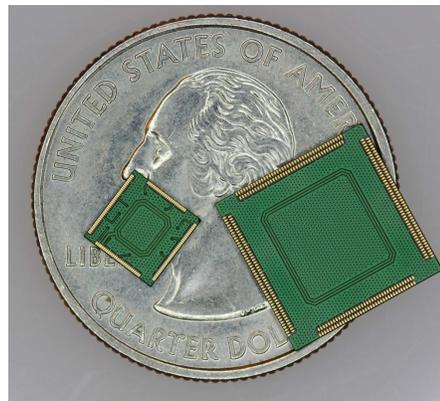


Figure 4 HDI Redistribution Parts for the 7x7mm and 3x3 mm Die Suitable for Wire Bonding to LGA 484 and LGA 168 Ceramic Packages

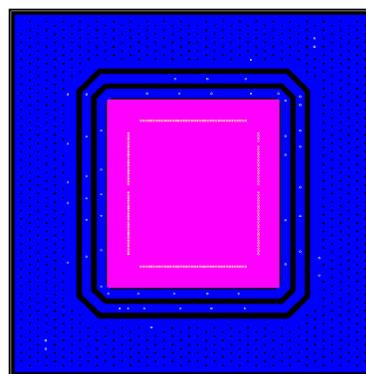


Figure 5 16x16 BGA Art Work Showing 7x7 mm Die Bond Sites and the Power and Ground Rings

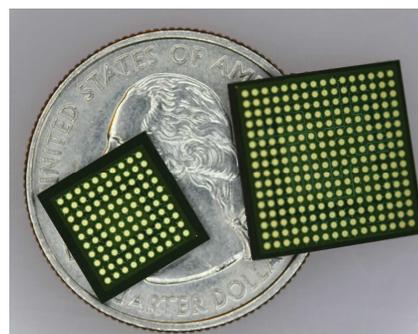


Figure 6 HDI BGA Parts for the 90nm 3x3mm and 7x7mm ASICs

HDI Structure and Process Flow

This section is based on the paper in [Gowda, 2012] and describes the HDI Structure and Process Flow. The main

feature of HDI technology (also referred to as POL for Power Overlay) is a planar, copper interconnection structure, using vias through a polyimide adhesive layer to make direct connection to the die contact pads. This interconnect structure replaces conventional wire bonds and flip chip interconnects. The technology offers significantly reduced parasitic inductance and resistance, while providing a thin profile, higher density packaging and the ability to interconnect active and passive devices of significantly different feature sizes with a single interconnect platform. Multiple interconnect layers can be built-up as needed with the option to co-fabricate passive elements such as inductors, resistors, and capacitors within the process flow. The technology also allows for embedding die completely in an ultra thin structure with dual-side I/Os. The platform leverages standard equipment and processes used in semiconductor fabrication, PCB fabrication, and surface mount assembly.

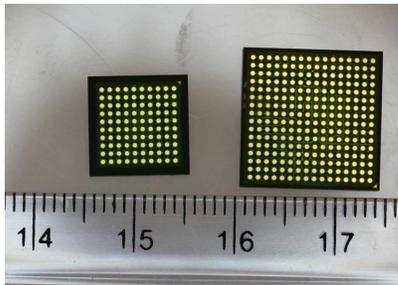


Figure 7 Parts for the 90nm 3x3mm and 7x7mm ASICs. (Ruler in mm).

Figure 8 shows the cross-section of a typical POL Cu via, through a dielectric layer composed of a polyimide and adhesive, made directly to the die bond pads where a highly reliable metallurgical joint can be obtained with standard die metallization (Al, Cu, etc.). As illustrated in Figure 8, POL Cu interconnects replace conventional wire bonds with an array of vias to the die and metal lines on the polyimide that are spatially arranged to conform to the device-type and contact pad geometry and are designed with electrical, thermal, and mechanical functionality in mind.

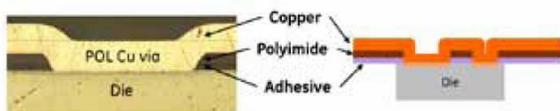


Figure 8 Basic one layer representation of POL (HDI) Interconnect

Figure 9 illustrates a generic version of a one-polyimide-layer POL process flow. The dielectric film (typically polyimide) is stretched over a metal frame and is the foundation on which the modules are constructed. These frames can be of many sizes and are designed to provide dimensional stability throughout the fabrication process. After the application of an adhesive layer, the devices are

placed on the adhesive layer and cured. Vias are then formed through the polyimide adhesive layers using a laser-drilling/ ablation process to expose the device bond pads. Finally, the POL Cu interconnect layer is metallized and patterned to form the interconnects. A metal layer can also be applied on the die side of the polyimide layer to provide a second layer of routing or added functionality. For multiple layers, the process of lamination of a polyimide layer with an adhesive, drilling, and metallization are repeated. Depending on the diameter of the vias, they can be formed before or after the attachment of the die. For large via sizes (125µm and higher) as used for typical power devices, via openings can be formed using a laser before attachment of the die and for smaller vias (125µm and smaller, typically for ICs), via openings are formed after the attachment of the die through a via ablation process. Depending on the electrical/RF performance, routing density, device pad sizes, and reliability requirements, the dielectric materials and thickness (13µm to 125µm), copper thickness (4µm to 150µm), via sizes (25µm to 2.5mm), line width and spacing (down to 25µm, depending on Cu thickness), and layer count required are used. These process steps are foundational to the POL packaging platform and constitute the “1st - level” interconnection scheme. Depending on the die/module type and application, the rest of the process can include the attachment to a substrate and encapsulation. In the case of an embedded system, the layers on the front side are replicated on the back side to form a balanced double-sided structure.

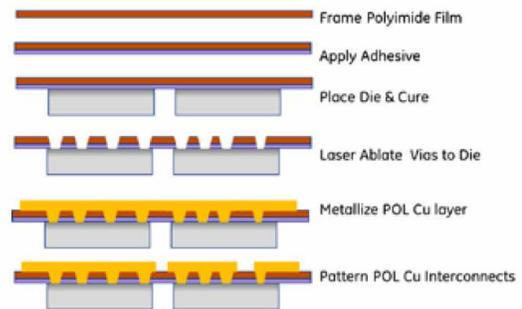


Figure 9 Schematic illustration of a POL intelligent power module (IPM)

Parallel Non Volatile Memory (NVM) to SPI Conversion Multi-Chip Module (MCM)

With the above overview of HDI, we address a third challenge for reducing size and part count. With the HDI process we can embed multiple Die into a single part. A particularly important application for achieving small size, low power and weight is to convert existing Radiation Hardened Parallel Non Volatile Memory (NVM) die to support the SPI serial interface. For the Rad Hard ASICs that support SPI bootstrap to copy the code from a NVM

device to on-chip SRAM, a single part for the SPI NVM paves the way for miniaturized, low power, high performance Radiation Hardened Microcontrollers in Space. Currently SPI based Rad Hard NVM do not exist for 300 kRad(Si) and 1 MRad(Si). To this end, Micro-RDC has designed a 3x3mm Radiation Hardened ASIC to interface to existing parallel NVMs to convert them to a SPI Slave interface. Figure 10 shows the three chip solution to booting up the ASIC SoC's from Parallel NVM. In Figure 11, we show a solution with HDI which embeds the 3x3 mm ASIC and the Parallel NVM Die into a single part. This results in a dramatic reduction of pin count and size and weight reduction. Note that the 3x3mm ASIC SPI interface chip uses Temporal Latch technology which make the logic immune to SEU.

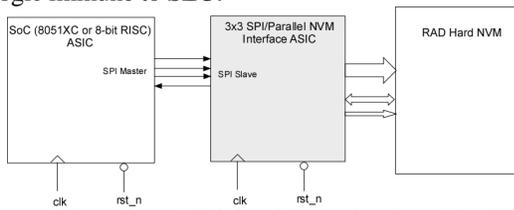


Figure 10 Interface ASIC for Converting Parallel NVM to SPI Interface.

Thus we anticipate the introduction of further HDI parts that will enable Space Missions in the most harsh environments especially with TID hardness above 1 MRad (Si).

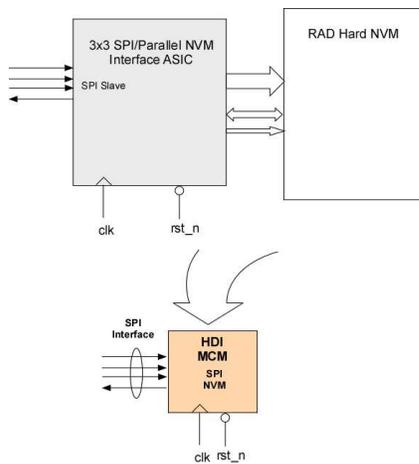


Figure 11 HDI Solution to Miniaturized Rad Hard SPI NVM

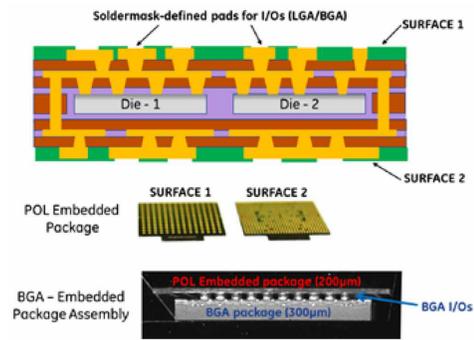


Figure 12 Embedded die package with POL(HDI) interconnects

Summary

In summary, the HDI process allows for complex designs in the 90nm, 45nm and 32 nm technology nodes to be packaged for space borne applications meeting the demands for high density logic, speed, low power and small size and weight while also accommodating the higher pin counts. In addition, with the BGA HDI solutions, we meet the requirements for reliability and survival in the harsh environments encountered in spaceborne applications [Ader, 1991],[Ghaffarian,2005] including ultra high acceleration [Mars Microprobe Mission. 1999] and temperature cycling.

Acknowledgements

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